**SCHOOL OF ENGINEERING**

**DEPARTMENTOF ELECTRONICSANDCOMMUNICATIONENGINEERING**

AReport

## One week SDP on

# "FPGA Design Acceleration through IP core on 28/04/2025-02/05/2025"

The chip crafters club under the Research Group NIVAG-Dept of ECE successfully conducted a week workshop on"**FPGA Design Acceleration through IP core**" for III B.Tech students from 28th April 2025 to 2nd May 2025. This workshop aims to provide insights into the importance of XILINX and CADENCE tool for student development in the fields of VLSI. This workshop comprises of theoretical lectures and demonstrations of the software and various toolboxes by department faculties.

The Student Development Program (SDP) on "FPGA Design Acceleration through IP Core" was conducted with the objective of imparting practical knowledge and hands-on skills in modern digital system design using Field Programmable Gate Arrays (FPGAs). The focus was on accelerating the FPGA design process through the effective use of Intellectual Property (IP) cores, enabling students to achieve faster development cycles and higher design efficiency.

Totally 42 students participated in the workshop and it was organized in association with **the IETE Student Forum (ISF).**

**Mr.K.Srinivas, Mrs.K.Thrisandhya,** worked as Faculty Coordinators for this workshop.

**Day-1 (28 April 2025) INAUGURATION (9:45amto11 am):**

The workshop was inaugurated by Director, Dean-School of Engineering, and ECE-Head at the ECE seminar hall from 9:45 am to 11 am.

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**DEPARTMENTOF ELECTRONICSANDCOMMUNICATIONENGINEERING**

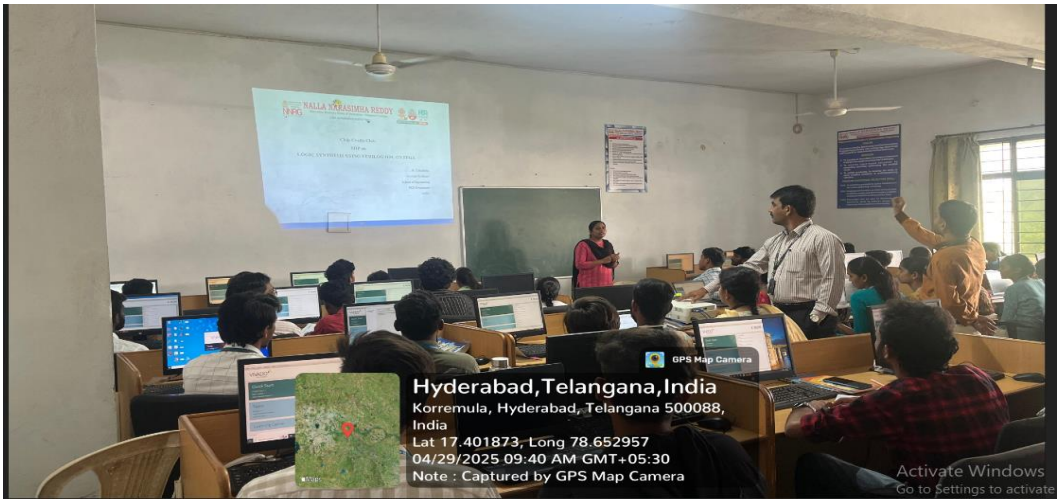
**Day-1 Forenoon (11:15amto12:50pm) and Afternoon (1:30pmto4:00pm):**

The workshop started from forenoon session 2 in which **Mrs.K.Thrisandhya** delivered the lecture on **"Combinational design using HDL"** and related concepts.


**Mrs.K.Thrisandhya,** Assistant Professors resource person delivered the concepts of **"Combinational circuits"**

**Day2 (29 April 2025) Forenoon Session 1:**

In the morning session, **Mrs.K.Hemalatha** handled the theoretical session on **"Sequential Design using HDL" ,** students will learn the concepts of latches ,flip-flops and registers which will help them to learn more about the larger circuits.




**Mrs.K.Hemalatha**, Assistant Professor of ECE, as a resource person delivered the **concept of sequential circuits.**

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**DEPARTMENTOF ELECTRONICSANDCOMMUNICATIONENGINEERING**

**Day2 (29 April 2025) afternoon Session 2:**

In the session2, **Mrs.V.V.Nandini** handled hands on session on **"Implementation of sequential circuits Design on FPGA",** students learned the importance of implementation of the logic circuits on to the advance boards like FPGA and CPLD boards**.**


**Mrs.V.V.Nandini,** Assistant Professor session on **Implementation of sequential circuits Design on FPGA**

**Day3 (30 April 2025) forenoon Session 1:**

In the Session 3 "**Hands on Session on IP Core using HDL**" by **Dr.B.Hariprasad Naik and Mrs.V.V.Nandini** in which the students will which bridge the gap between theory and real-world application like the following skills will be provides

1. Practical HDL Skills- Work with real, complex modules using HDL
2. Industry Readiness- IP core experience is valued in VLSI/FPGA jobs
3. Better Understanding- Understand modularity, reuse, and hierarchy
4. Simulation & Debugging Skills- Gain hands-on verification experience
5. Real Hardware Exposure- Learn how IPs are mapped to FPGAs.

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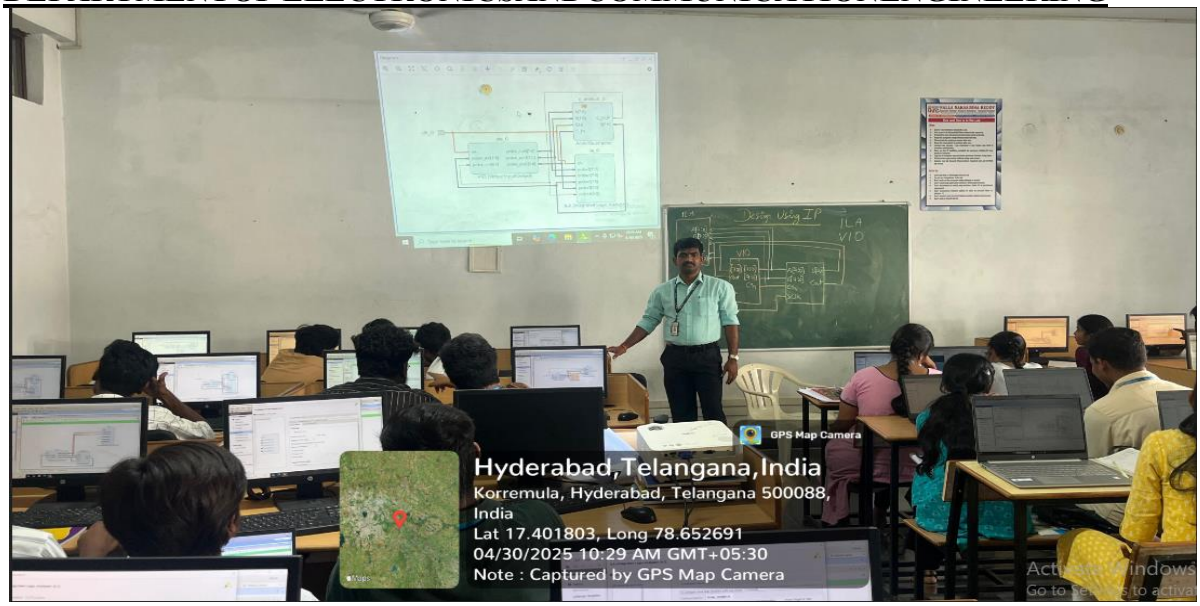


**Dr.B.Hariprasad Naik** Assistant Professor of ECE, delivered lecture on **Hands on Session on IP Core using HDL**

**Day3 (30 April 2025) afternoon Session 2:**

The hands-on session has been continued by the Chip crafters club faculty members.


Handson session on IP CORE by **Mrs.K.Hemalatha** and **Mrs.V.V.Nandini**

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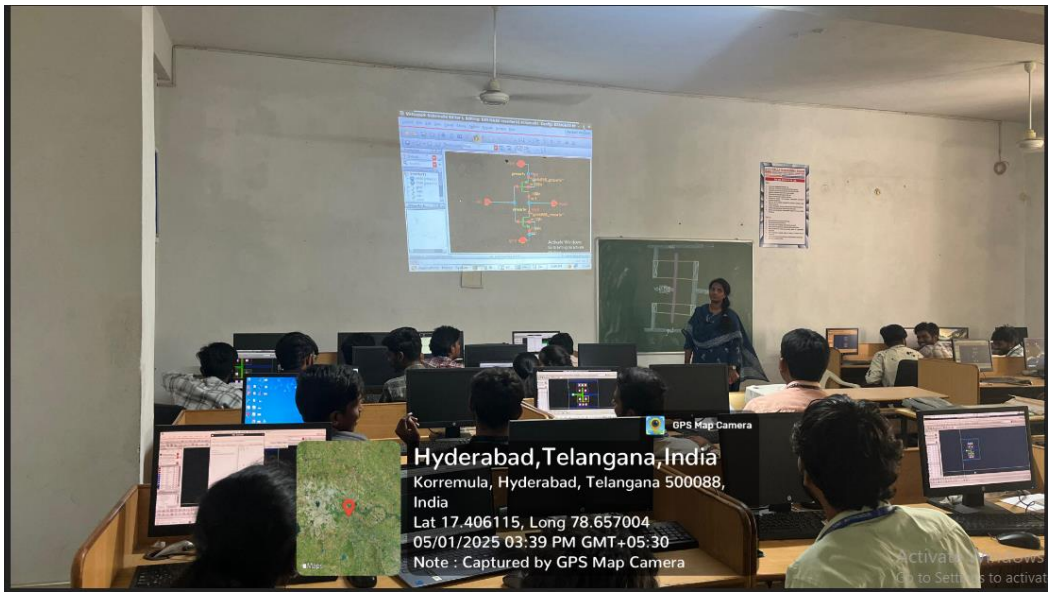
## DEPARTMENTOF ELECTRONICSANDCOMMUNICATIONENGINEERING

**Day-4 (1st May 2025) forenoon Session1:**

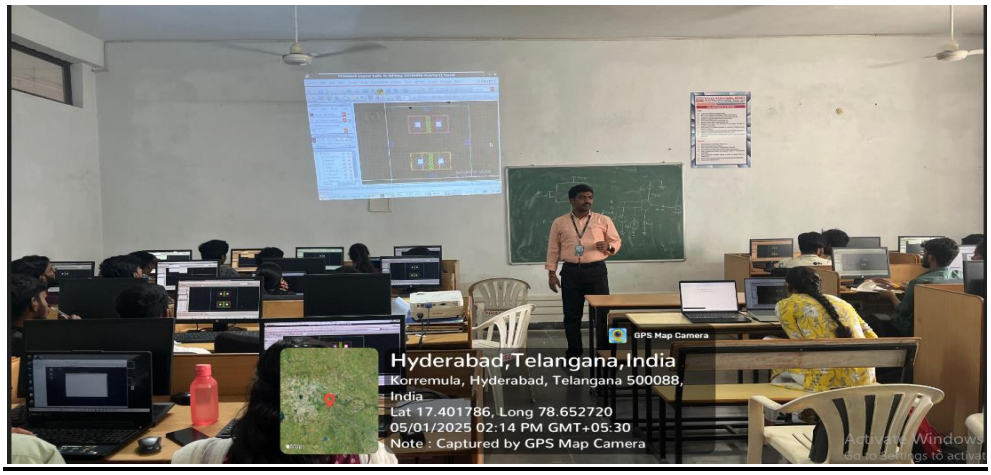
In the morning session, resource person **Mrs.V.V.Nandini** delivered a lecture on **"**Implementation of Digital Circuits using Cadence Virtuoso "student's learned about how to implement the logic circuits using cadence tool which includes simulation and layout which is very much useful for real world scenario.




Session by **Mrs.V.V.Nandini** on Implementation of logic **gates in cadence physical designing.**

**Day-4(1st may 2025) forenoon Session2:**

Sessionis handled by resource person Dr.B.Hariprasad Naik delevers the topic of Implementation of Digital Circuits using Cadence Virtuoso which includes layout implementations.




Session by **Dr.B.Hariprasad Naik** on **LAYOUT implementation of basic logical blocks**.

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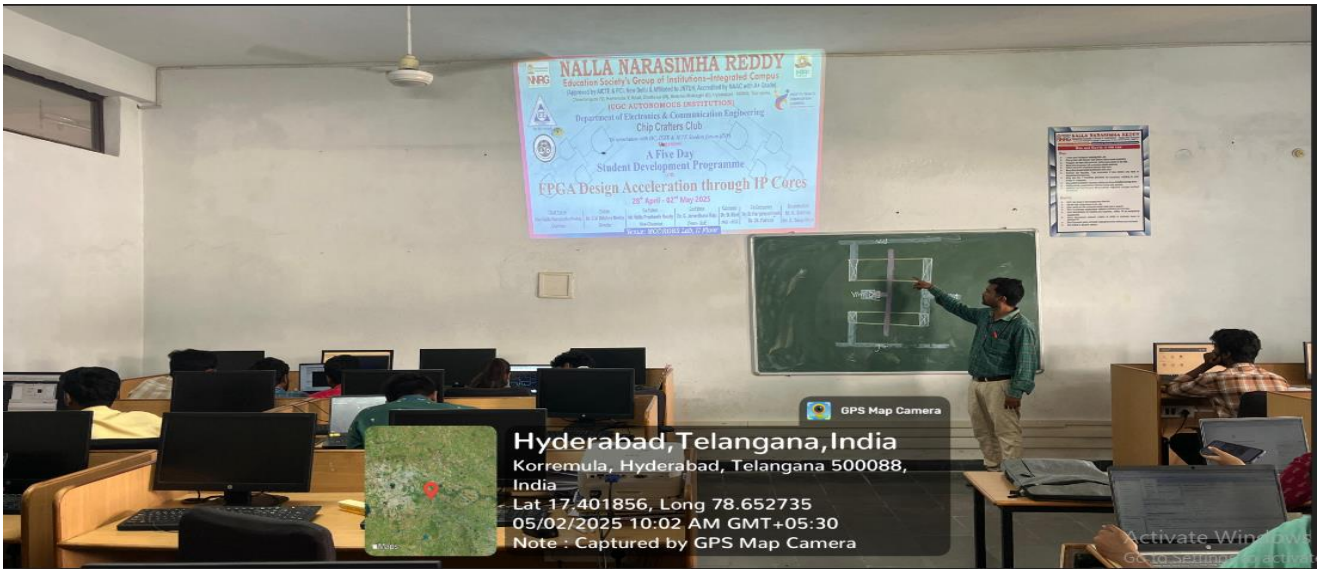
**Day 5(2nd May 2025) forenoon session 1:**

In the morning session, resource person **Mr. Srinivas** delivered a lecture on**" Implementation of VLSI logic circuits**" and students developed advanced digital logic designs which includes their projects in this domain.




Lecture on **Implementation of Advanced logic designs** by **Mr.Srinivas**.

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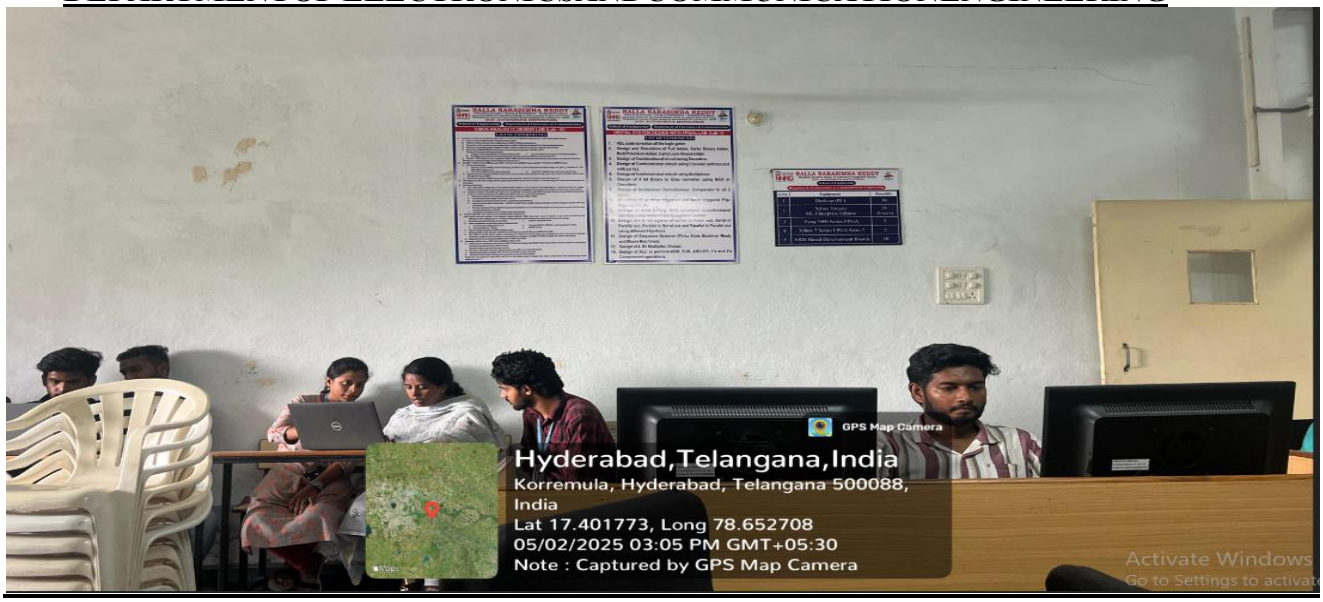


**Hands-on session** by Mrs.**V.V.Nandini.**

## Outcomes of the Workshop

### 1. Development Program Outcomes (DPOs):

| DPO Code | Development Program Outcome Description |
|---|---|
| DPO1 | Understand the fundamentals of combinational and sequential circuits. |
| DPO2 | Acquire skills to develop custom IP cores and integrate existing IP cores into FPGA-based by standard tools like Vivado. |
| DPO3 | Apply innovative thinking to design and deploy real-time applications |
| DPO4 | Gain awareness of current industry trends and standards in modern communication systems. |
| DPO5 | Enhance their ability to work in teams and communicate design processes and outcomes |

## 2. Mapping of DPOs to POs, PSOs, and PEOs

| DPO Code | Mapped PO(s) | Mapped PSO(s) | Mapped PEO(s) | Justification |
|---|---|---|---|---|
| DPO1 | PO1, PO3 | PSO1, PSO2 | PEO1 | Aligns with foundational understanding and technological updates in modern communication. |
| DPO2 | PO4, PO5 | PSO1, PSO2 | PEO2 | Encourages technical practice and use of tools to solve problems. |
| DPO3 | PO1, PO3, PO11 | PSO2 | PEO2, PEO3 | Fosters innovation and leadership in addressing engineering challenges. |
| DPO4 | PO6, PO12 | PSO1 | PEO1 | Promotes awareness of societal trends and continuous learning. |
| DPO5 | PO9, PO10 | PSO2 | PEO3 | Develops communication and team skills essential for ethical and effective practice. |